Abstracts

Enhancement-Mode GaAs MESFET Technology for Low Consumption Power and Low Noise Applications (Dec. 1994, Part II [T-MTT])

S. Nakajima, K.-I. Matsuzaki, K. Otobe, H. Nishizawa and N. Shiga. "Enhancement-Mode GaAs MESFET Technology for Low Consumption Power and Low Noise Applications (Dec. 1994, Part II [T-MTT])." 1994 Transactions on Microwave Theory and Techniques 42.12 (Dec. 1994, Part II [T-MTT] (1994 Symposium Issue)): 2517-2523.

Ion-implanted enhancement-mode GaAs MESFET's with an advanced Lightly Doped Drain (LDD) structure have been developed for low cost, low consumption power, and low noise applications. The advanced LDD structure, which consists of step graded (n+, n', n') source/drain implanted regions and surrounding p-layers located within the n/sup +/ -layers, is effective to suppress the short channel effects and reduce source/drain parasitic resistance without increasing the parasitic capacitance. A manufacturable self-aligned process based on a dummy gate has also been developed for the fabrication of this structure. The 0.3 µm devices show a noise figure of less than 1 dB with an associated gain of higher than 9 dB at 6 GHz, even at 1 mW operation. Furthermore, standard deviations of noise figure and associated gain are as small as 0.05 dB (at an average of 0.83 dB) and 0.32 dB (at an average of 8.82 dB), respectively, under a 1 mW operation over a 3"Phi wafer.

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